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| EXAMINER | | | | |
| DAO, THUY CHAN | | | | |
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/720,614

Applicant(s)

RAMMEL, MARTIN G.

Examiner

Thuy Dao

Art Unit

2192

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 September 2008.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 17 and 31-37 is/are pending in the application.
4a) Of the above claim(s) 1-7, 9, 12-16, 18, 27 and 28 is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 17 and 31-37 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 24 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____

DETAILED ACTION

1. This action is responsive to the amendment filed on September 2, 2008.
2. Claims 17 and 31-37 have been examined.

Response to Amendments

3. In the instant amendment, claims 17 have been amended; claims 1-7, 9, 12-16, 18, and 27-28 have been canceled; and claims 31-37 have been added.
4. The objection to claim 19 is withdrawn in view of Applicant's amendments.

Claim Objections

5. Claims 31, 32, and 35 are objected to because of minor informalities. Acronyms in claims 31 and 32 should be spelled out at the first appearance in claims.

Claim 31:

Line 1, the phrase is considered to read as - -... with a [[CPU]] central processing unit (CPU) and an [[FPGA]] Field Programmable Gate Array (FPGA)- -.

Claim 32:

Line 3, the phrase is considered to read as - -[[FFT]] Fast Fourier Transform (FFT)- -.

Claim 35:

Line 1, the phrase is considered to read as - -[[Apparatus]] An apparatus comprising: - -.

Appropriate correction is requested.

Response to Arguments

6. Applicants' arguments have been considered. but are moot in view of the new ground(s) of rejection.

Claim Rejections – 35 USC §102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claim 31 is rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,883,147 to Ballagh (art made of record, hereafter "Ballagh").

Claim 31 (new):

Ballagh discloses *a method of performing a numerical simulation with a CPU and an FPGA, comprising:*

using the CPU (e.g., FIG. 2, processor 204, col.5: 1-38)

to perform a numerical simulation including generating input signals (e.g., col.5: 29-38; col.3: 52-65) and

sending the input signals to the FPGA (e.g., FIG. 2, sending the input signals to FPGA 202 including peripheral component 210, which may be FIR filter 250 in FIG. 3A and/or FIR filter and data path 260 in FIG. 3B, col.5: 19-28);

using the FPGA to apply a model to the input signals and send results of the model back to the CPU (e.g., FIG. 4A, generating a model for peripheral component 210, col.6: 47-65),

the FPGA also generating a first output that marks data as valid or invalid (e.g., FIG. 3A, FPGA 202 generating "coef_we" (first output) to mark "coef" valid or invalid and sending "coef_we" to its sub-component FIR filter 250, col.5: 55-65),

a second output that indicates the first sample of each frame (e.g., FIG. 3A, output port "yn" indicating data in output frames, col.5: 29-38 and 43-48), and

a third output that indicates when the model can accept data (e.g., FIG. 3A, FPGA 202 generating "rfd" indicating status "busy" or not, col.5: 55-65); and

wherein the CPU uses the results in the numerical simulation and the outputs to maintain data flow with the FPGA (e.g., FIG. 2, col.4: 65 – col.3: 38).

Claim Rejections – 35 USC §103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claims 32-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ballagh in view of APA (art of record, Admitted Prior Art).

Claim 32 (new):

Ballagh does not explicitly disclose *the method of claim 31, wherein the input signals include sine wave functions representing real and imaginary inputs; and wherein the model includes a FFT.*

However, in an analogous art, APA further discloses *the input signals include sine wave functions representing real and imaginary inputs; and wherein the model includes a FFT (e.g., page 2: 4-23).*

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine APA's teaching into Ballagh's teaching. One would have been motivated to do so to transform a digitized waveform in the time domain into a digital representation in the frequency domain using Simulink simulation software as suggested by APA (e.g., page 2: 5-9 and 20-23).

Claim 33 (new):

Ballagh discloses *the method of claim 32, wherein the FPGA converts inputs from double point precision to fixed point prior to performing the transform* (e.g., col.3: 52-65; col.5: 29-38); and

wherein the FPGA converts the results from fixed point back to double precision prior to sending the results back to the CPU (e.g., col.4: 65 – col.5: 38; col.6: 47-65).

APA further discloses *the input signals include sine wave functions representing real and imaginary inputs; and wherein the model includes a FFT* (e.g., page 2: 4-23).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine APA's teaching into Ballagh's teaching. One would have been motivated to do so to transform a digitized waveform in the time domain into a digital representation in the frequency domain using Simulink simulation software as suggested by APA (e.g., page 2: 5-9 and 20-23).

Claim 34 (new):

APA further discloses *the method of claim 32, wherein the CPU performs a numerical simulation of a radar system* (e.g., page 2: 4-15).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine APA's teaching into Ballagh's teaching. One would have been motivated to do so to as set forth above.

Claim 35 (new):

Ballagh discloses *an apparatus* which recite(s) the same limitations as those of claim 31, wherein all claimed limitations have been addressed and/or set forth above. Therefore, as the reference teaches all of the limitations of the above claim(s), it also teaches all of the limitations of claim 35.

APA further discloses *a numerical simulation of sine wave functions representing real and imaginary inputs; and performing an FFT on the inputs* (e.g., page 2: 4-23).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine APA's teaching into Ballagh's teaching. One would have been motivated to do so to transform a digitized waveform in the time domain into

a digital representation in the frequency domain using Simulink simulation software as suggested by APA (e.g., page 2: 5-9 and 20-23).

Claim 36 (new):

Ballagh discloses *the apparatus of claim 35, wherein the FPGA converts the real and imaginary inputs from double point precision to fixed point prior to performing the transform* (e.g., col.5: 1-38; col.6: 47-65); *and*

wherein the FPGA converts the results of the FFT from fixed point back to double precision prior to sending the results back to the CPU (e.g., col.3: 52-65; col.4: 65 – col.5: 38).

Claim 37 (new):

APA further discloses *the apparatus of claim 35, wherein the CPU performs a numerical simulation of a radar system* (e.g., page 2: 4-15).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine APA's teaching into Ballagh's teaching. One would have been motivated to do so to as set forth above.

11. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ballagh in view of APA and US Patent No. 7,110,935 to Hwang et al. (art made of record, hereafter "Hwang").

Claim 17:

Ballagh discloses *the method of Claim 32, wherein the FPGA is programmed to perform steps including:*

performing receiving the real and imaginary inputs at first and second inputs of an FFT block via a pair of gateway in blocks (e.g., FIG. 1B, col.5: 4-17);

coupling an output of a double delay block to a third input of the FFT block, the third input being adapted to mark data input as valid or invalid (e.g., col.3: 27 – col.4: 29);

coupling an output of a $k=0$ block to a fourth input of the FFT block, the fourth input being adapted to control a forward or a reverse transform (e.g., FIG. 2, col.5: 17 – col.6: 15);

coupling outputs of FFT block to at least one D flip flop-based registers adapted to provide a signal latency; and coupling the outputs of the registers to at least one gateway out (e.g., FIG. 3B, elements 252 and 260, col.8: 23-49).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Hwang's teaching into Ballagh and APA's teaching. One would have been motivated to do so to provide system and target libraries as suggested by Hwang (e.g., col.3: 27 – col.4: 9).

Conclusion

12. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

13. Any inquiry concerning this communication should be directed to examiner Thuy Dao (Twee), whose telephone/fax numbers are (571) 272 8570 and (571) 273 8570, respectively. The examiner can normally be reached on every Tuesday, Thursday, and Friday from 6:00AM to 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam, can be reached at (571) 272 3695.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273 8300.

Any inquiry of a general nature of relating to the status of this application or proceeding should be directed to the TC 2100 Group receptionist whose telephone number is (571) 272 2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thuy Dao/
Examiner, Art Unit 2192

/Tuan Q. Dam/
Supervisory Patent Examiner, Art Unit 2192